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SCOPE

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Electronics & Instrumentation Engineering

Department of Electronics & Instrumentation Engineering
KAKATIYA INSTITUTE OF TECHNOLOGY & SCIENCE
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(An Autonomous Institute under Kakatiya University, Warangal)

DEPARTMENT OF ELECTRONICS & INSTRUMENTATION ENGINEERING
KAKATIYA INSITUTE OF TECHNOLOGY & SCIENCE: WARANGAL-15

VISION

To provide quality education in Electronics & Instrumentation Engineering by nurturing the students with strong technical, analytical, practical skills and ethics to make them engineering professionals who cater to the societal needs with a high degree of integrity and social concern.

MISSION

1. To provide progressive and quality educational environment with the help of dedicated faculty and staff by fully utilizing the information technology aiming at continuous teaching and learning process.

2. To produce engineering graduates fit for employability with a competence to design, develop, invent and solve instrumentation engineering problems.

3. To make the students ethically strong by inculcating sense of brotherhood.

4. To make the students research oriented by providing latest technical knowledge and thus cater to the changing needs of industry and commerce.

EDITORIAL BOARD

PREFACE

This magazine summarizes the current state of Electronics and Instrumentation Engineering, providing an arena for the student community to showcase their technical talents in a great way. Keeping in view of the present era of technological revolution in the field of Instrumentation Engineering, the students of E&IE department, KITS Warangal presents you **SCOPE**.

We acknowledge the essential contribution of the reviewers, whose efforts are deeply appreciated.

We feel that such technical magazine is very well required as it helps in updating the knowledge of future engineers.

The Department of E&IE is very much thankful to the Management for their continuous support and encouragement for making the Technical Magazine **SCOPE**.

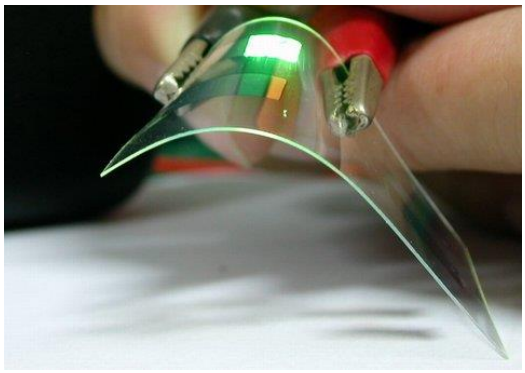
CONTENTS

CHAPTER 1: OLED TECHNOLOGY

1.Introduction

Organic light emitting devices (OLEDs) operate on the principle of converting electrical energy into light, a phenomenon known as electroluminescence. They exploit the properties of certain organic materials which emit light when an electric current passes through them. In its simplest form, an OLED consists of a layer of this luminescent material sandwiched between two electrodes. When an electric current is passed between the electrodes, through the organic layer the light emitted by an OLED, atleast one of the electrodes must be transparent.

When OLEDs are used as pixels in flat displays they have some advantages over backlit active-matrix LCD displays – greater viewing angle, lighter weight, and quicker response. Since only the part of the display that is actually lit up consume power, the most efficient OLEDs available today use less power.



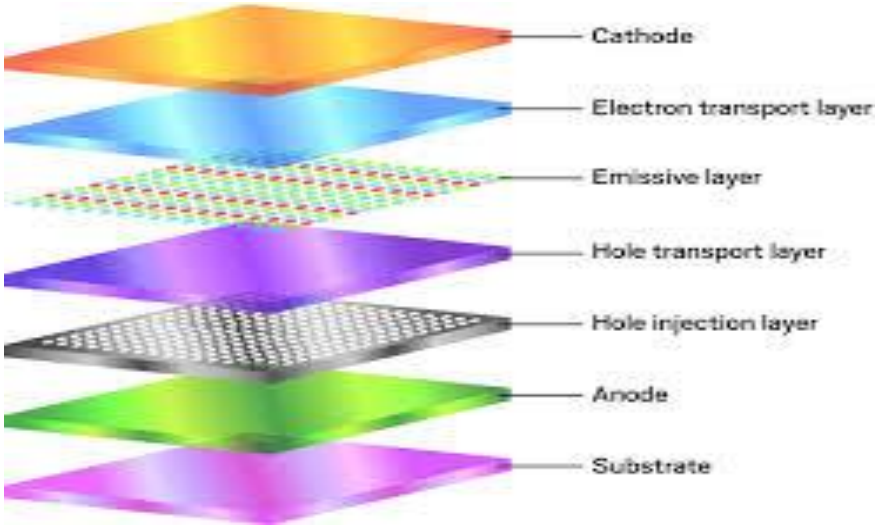
Many major electronic companies, such as Philips and Pioneer, are today investing a considerable amount of money in the science of organic electronic and optoelectronic devices.

2.Components of OLED

The components in an OLED differ according to the number of layers of the organic material. There is a basic single layer OLED, two layer and also three layer OLED's. As the number of layers increase the efficiency of the device also increases. The increase in layers also helps in

injecting charges at the electrodes and thus helps in blocking a charge from being dumped after reaching the opposite electrode. Any type of OLED consists of the following component

1. An emissive layer
2. A conducting layer
3. A substrate
4. Anode and cathode terminals.



- SUBSTRATE- The substrate supports the OLED.

  Example: clear plastic, glass, foil.
- ANODE- The anode removes electrons when current flows through the device.
  Example: indium tin oxide

- ORGANIC LAYERS- These layers are made of organic molecules or polymers.
  - CONDUCTIVE LAYER- This layer is made of organic plastic molecules that send electrons out from the anode.
    Example: polyaniline, polystyrene

  - EMISSIVE LAYER- This layer is made of organic plastic molecules (different ones from the conducting layer) that transport electrons from the cathode; this is where light is made.
    Example: polyfluorine, Alq3
- CATHODE- The cathode injects electrons when a current flows through the device. (It may or may not be transparent depending on the device)
  Example: Mg, Al, Ba.

3.WORKING

Working principle:

As previously mentioned, OLEDs are an emissive technology, which means they emits light instead of diffusing or reflecting a secondary source, as LCDs and LEDs currently do. Below is a graphic explanation of how the technology works

4.CONCLUSION

Performance of organic LEDs depend upon many parameters such as electron and hole mobility, magnitude of applied field, nature of hole and electron transport layers and excited life-times. Organic materials are poised as never before to transform the world IF circuit and display technology. Major electronics firms are betting that the future holds tremendous opportunity for the low cost and sometimes surprisingly high performance offered by organic electronic and optoelectronic devices. Organic Light Emitting Diodes are evolving as the next generation of light sources. Presently researchers have been going on to develop a 1.5 emitting device. This wavelength is of special interest for telecommunications as it is the low-loss wavelength for optical fibre communications. Organic full-colour displays may eventually replace liquid crystal displays for use with lap top and even desktop computers. Researches are going on this subject and it is sure that OLED will emerge as future solid state light source.

#P. SHRAVANI
(III/IV)

CHAPTER 2: HAPTIC TECHNOLOGY

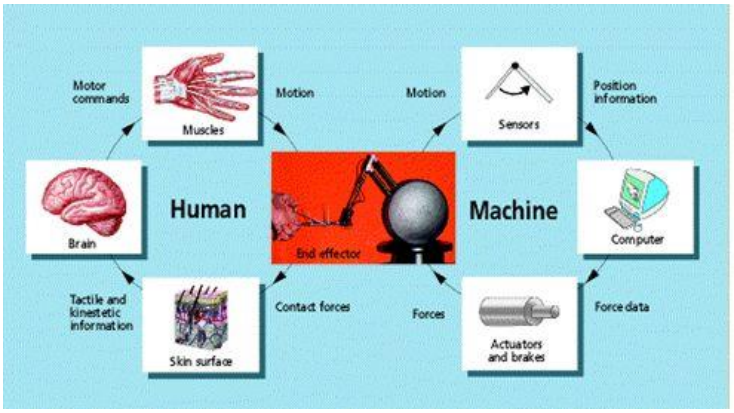
1. Introduction

Haptic technology refers to technology that interfaces the user with a virtual environment via the sense of touch by applying forces, vibrations, and/or motions to the user. This mechanical stimulation may be used to assist in the creation of virtual objects (objects existing only in a computer simulation), for control of such virtual objects, and to enhance the remote control of machines and devices (teleoperators). This emerging technology promises to have wide reaching applications as it already has in some fields. For example, haptic technology has made it possible to investigate in detail how the human sense of touch works by allowing the creation of carefully controlled haptic virtual objects. These objects are used to systematically probe human haptic capabilities, which would otherwise be difficult to achieve. These new research tools contribute to our understanding of how touch and its underlying brain functions work. Although haptic devices are capable of measuring bulk or reactive forces that are applied by the user, it should not to be confused with touch or tactile sensors that measure the pressure or force exerted by the user to the interface.

The term haptic originated from the Greek word (haptikos) meaning pertaining to the sense of touch and comes from the Greek verb ἅπτεσθαι (haptesthai) meaning to "contact" or "touch.

2. Working of haptics

Basic system configuration



Basically a haptic system consist of two parts namely the human part and the machine part. In the figure shown above, the human part (left) senses and controls the position of the hand, while the machine part (right) exerts forces from the hand to simulate contact with a virtual object. Also both the systems will be provided with necessary sensors, processors and actuators. In the case of the human system, nerve receptors performs sensing, brain performs processing and muscles performs actuation of the motion performed by the hand while in the case of the machine system, the above mentioned functions are performed by the encoders, computer and motors respectively.

3. Haptic devices

A haptic device is the one that provides a physical interface between the user and the virtual environment by means of a computer. This can be done through an input/output device that senses the body's movement, such as joystick or data glove. By using haptic devices, the user can not only feed information to the computer but can also receive information from the computer in the form of a felt sensation on some part of the body. This is referred to as a haptic interface. These devices can be broadly classified into:-

3.1 Virtual reality/ Tele-robotics based devices:-

- Exoskeletons and Stationary device
- Gloves and wearable devices
- Point-source and Specific task devices
- Locomotion Interfaces

3.2 Feedback devices:-

- Force feedback devices
- Tactile displays

4. Conclusion

Finally we shouldn't forget that touch and physical interaction are among the fundamental ways in which we come to understand our world and to effect changes in it. This is true on a developmental as well as an evolutionary level. For early primates to survive in a physical world, as Frank Wilson suggested, "a new physics would eventually have to come into this their brain, a new way of registering and representing the behavior of objects moving and changing under the control of the hand. It is precisely such a representational system—a syntax of cause and effect, of stories, and of experiments, each having a beginning, a middle,

and an end— that one finds at the deepest levels of the organization of human language." Our efforts to communicate information by rendering how objects feel through haptic technology, and the excitement in our pursuit, might reflect a deeper desire to speak with an inner, physically based language that has yet to be given a true voice.

#V. SREESHA

(III/IV)

CHAPTER 3: SWARM ROBOTICS

1. Introduction:

The research progress of swarm robotics is reviewed in details. The swarm robotics inspired from nature is a combination of swarm intelligence and robotics, which shows a great potential in several aspects. First of all, the cooperation of nature swarm and swarm intelligence are briefly introduced, and thespecial features of the swarm robotics are summarized compared to a single robot and other multi-individual systems. Then the modeling methods for swarm robotics are described, followed by a list of several widely used swarm robotics entity projects and simulation platforms. Finally, as a main part of this paper, the current research on the swarm robotic algorithms are presented in detail, including cooperative control mechanisms in swarm robotics for flocking, navigating and searching applications.

2. From nature swarm to swarm intelligence

2.1. Cooperation of nature swarms

Most swarm intelligence researches are inspired from how the nature swarms, such as social insects, fishes or mammals, interact with each other in the swarm in real life. These swarms range in size from a few individuals living in the small natural areas to highly organized colonies that may occupy the large territories and consist of more than millions of individuals. The group behaviors emerging in the swarms show great flexibility and robustness, such as path planning, nest constructing, task allocation and many other complex collective behaviors in various nature swarm .

The individuals in the nature swarm shows very poor abilities, yet the complex group behaviors can emerge in the whole swarm, such as migrating of bird crowds and fish schools, and foraging of ant and bee colonies as shown in Fig. 1. It's tough for an individual to complete the task itself, even a human being without certain experiences finds it difficultly, but a swarm of animals can handle it easily. Researchers have observed the intelligent group behaviors emerging from a group of individuals with poor abilities through local communication and information transmission.

Bacteria colonies

Bacteria often function as multicellular aggregates known as biofilms, exchanging the molecular signals for inter-cell communication. The communal benefits of multicellular cooperation include a cellular division of labor, collectively defending against antagonists, accessing more resources and optimizing the population survival by differentiating the distinct cell types. The resistance to antibacterial agents of the bacteria in the biofilms is 500 times more than that of individual bacteria of same kind.

Fish schools

Fish schools swim in the disciplined phalanxes and are able to stream up and down at impressive speeds and make a startling change in the shape of the school without collision as if their motions were choreographed. The fishes pay close attention to their neighbors when schooling with the help of eyes on the sides of heads and "schooling marks" on their shoulders. The fishes can benefit from fish schools in foraging and predator avoidance.

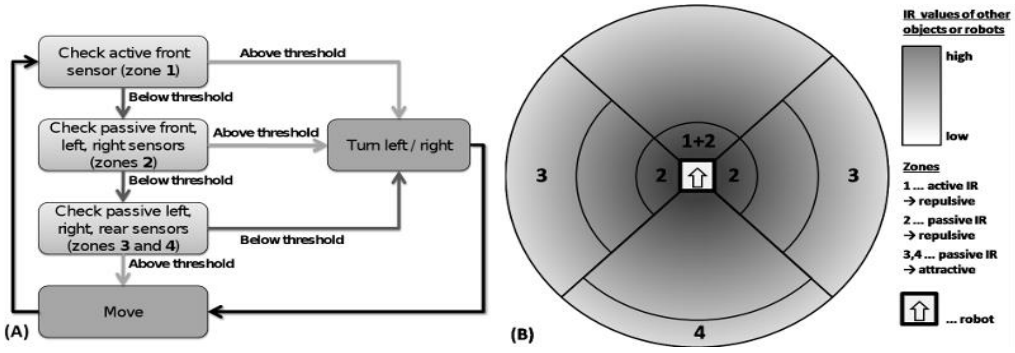
3.SWARM ROBOTICS ALGORITHMS

3.1 Flocking Algorithm:

Each robot in the swarm periodically emits IR-pulses. The robots then react (move straight ,turn left or turn right) depending on information from their active and passive IR-sensors. These sensors are polled periodically and the returned values are

then checked against predefined thresholds (Fig. 1B) in a simple subsumption architecture (Fig. 1A). First, the active IR-value for the front sensor is polled to find out whether there is an obstacle in front. If the value for the reflected IR-light is above a certain threshold, the robot turns away in a random direction. This is the basic collision avoidance of our robots. If there are no objects in its way, the robot checks the passive IR-values of all sensors. If the front, left or right sensor is above a certain threshold, the

Robot turns away from what is presumably another robot which is too close. This rule is usually referred to as the separation rule in flocking algorithms. If there is no other robot too close, the robot checks the passive IR-values of its left, right and rear sensors. For every sensor that returns a value that is a bove the environmental IR-light threshold but below the threshold which defines the maximally desired distance to another robot in that sector, the robot perfor ms a Basic vector addidtion and adds up all turns. It then decides to turn in a direction depending on whether there were more left or more right turns. Robots in the ear zone trigger a random turn reaction. This rule is usually referred to as the cohesion rule in flocking algorithms. The third rule in flocking algorithms is usually the alignment rule which generates the common direction of movement in a flock. Since we wanted our



A: Simple architecture depicting the flocking algorithm. The first decision results in collision avoidance, the second decision results in robot separation and the third decision results in flock cohesion and emergent alignment.

B: Simplified depiction of the perceived IR-values of other objects (reflected active IR) or flock mates(passive IR) dependent on their distance to the robot.

algorithm to be as simple as possible we wanted to exclude complex communication or image recognition procedures and implemented a method which generates emergent alignment. To achieve this we adjusted the thresholds for the cohesion rule so that robots tend to follow other robots. This is done by simply shifting the

threshold for the rear sensor more outwards in comparison to the thresholds for the left and right sensors (zones 3 and 4 in Fig. 1B). Depending on the position and heading of two approaching robots, one robot will be behind the other robot. When both robots move, the robot behind will turn towards the robot in front before the robot in front reacts and turns around. This creates a leader robot and a follower robot, purely by chance. These two robots will then move around in the arena without separating. If the path of these two robots is blocked by an obstacle or another robot joins the flock, the arrangement can change instantly. If two robots approach frontally, they will avoid each other, only to turn back to each other shortly after, which can create a deadlock situation. To prevent such situations, we implemented a random-turn reaction which means that robots will randomly turn either left or right when avoiding other robots in front.

4.Conclusion

- Robots are going to be an important part of the future.
- Robots as of now are either working in single hand system; whereas SWARM is and Multiple bot system.
- Having some electronic tools won't give a structured bot all we need is to design and place every part collectively, which in itself is a job of great minds.
- The swarm-bots have already succeeded in crossing ditches, transporting small heavy objects, and navigating rough terrain—none of which a single s-bot could have accomplished alone.
- This procedure is repeatedly applied until a termination criterion is satisfied.
- It's hard to imagine a future in which robots are not an integral part of our daily lives.

#I. NIHARIKA

(IV/IV)

CHAPTER 4: TRANSPARENT ELECTRONICS

1.Introduction

Transparent electronics is an emerging science and technology field focused on producing 'invisible' electronic circuitry and opto-electronic devices. Applications include consumer electronics, new energy sources, and transportation Other civilian and military applications in this research field include real-time wearable displays. As for conventional Si/III–V-based electronics, the basic device structure is based on semiconductor junctions and transistors.However, the device building block materials, the semiconductor, the electric contacts, and the dielectric/passivation layers, must now be transparent in the visible –a true challenge! Therefore, the first scientific goal of this technology must be to discover, understand, and implement transparent high-performance electronic materials. The second goal is their implementation and evaluation in transistor and circuit structures. The third goal relates to achieving application-specific properties since transistor performance and materials property requirements vary, depending on the final product device specifications. Consequently, to enable this revolutionary technology requires bringing together expertise from various pure and applied sciences, including materials science, chemistry, physics, electrical /electronic/circuit engineering, and display science.

During the past 10 years, the classes of materials available for transparent electronics applications have grown dramatically. Historically, this area was dominated by transparent conducting oxides because of their wide use in antistatic coatings, touch display panels, solar cells, flat panel displays, heaters ,defrosters, 'smart windows' and optical coatings.

All these applications use transparent conductive oxides as passive electrical or optical coatings. The field of transparent conducting oxide (TCO) materials has been reviewed and many treatises on the topic are available. However, more recently there have been tremendous efforts to develop new active materials for functional transparent electronics. These new technologies will require new materials sets, in addition to the TCO component, including conducting, dielectric and semiconducting materials, as well as passive components for full device fabrication.

2. Combining optical transparency with electrical

Conductivity

Transparent conductors are neither 100% optically transparent nor metallically conductive. From the band structure point of view, the combination of the two properties in the same material is contradictory: a transparent material is an insulator which possesses completely filled valence and empty conduction bands; whereas metallic conductivity appears when the Fermi level lies within a band with a large density of states to provide high carrier concentration. Efficient transparent conductors find their niche in a compromise between a sufficient transmission within the visible spectral range and a moderate but useful in practice electrical conductivity. This combination is achieved in several commonly used oxides – In2O3, SnO2, ZnO and CdO. In the undoped stoichiometric state, these materials are insulators with optical band gap of about 3 Ev. To become a transparent conducting oxide (TCO), these TCO hosts must be degenerately doped to displace the Fermi level up into the conduction band. The key attribute of any conventional n type TCO host is a highly dispersed single free electron- like conduction band (Figure 1). Degenerate doping then provides both

(i) the high mobility of extra carriers (electrons) due to their small effective mass and

(ii) low optical absorption due to the low density of states in the conduction band.

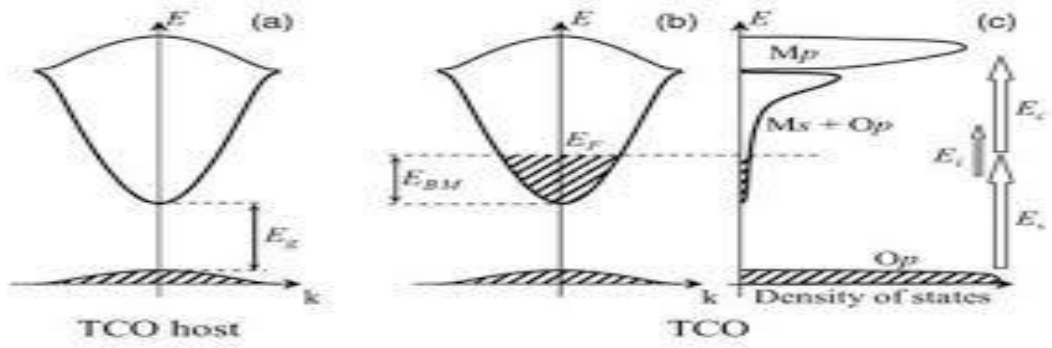


Fig.1: (a) Schematic electronic band structure of aTCOhost – an insulator with a band gap Eg and a dispersed parabolic conduction band which originates from interactions between metal s and oxygen p states. (b) and (c) Schematic band structure and density of states of a TCO, where a degenerate doping displaces the Fermi level (EF) via a Burstein-Moss shift, EBM, making the system conducting.

Achieving the optimal performance in a TCO is a challenging because of the complex interplay between the electronic and optical properties. The large carrier concentrations desired for a good conductivity may result in an increase of the optical absorption

(i)at short wavelengths, due to inter-band transitions from the partially filled conduction band and

(ii)at long wavelengths, due to intra-band transitions within this band. In addition, plasma oscillations may affect the optical properties by reflecting the electromagnetic waves of frequency below that of the plasmon. Furthermore, ionized impurity scattering on the electron donors (native point defects or substitutional dopants) have a detrimental effect on the charge transport, while the structural relaxation around the impurities may alter the electronic and optical properties of the host, leading to a nonrigid-band shift of the Fermi level. We demonstrate here that a thorough understanding of the microscopic properties of metal oxides provides an insight into the underlying phenomena and also suggests that the range of efficient TCO materials can be significantly broaded.

3.Transparent electronics devices:

In order to produce a transparent-electronics-based system, appropriate materials must be selected, synthesized, processed, and integrated together in order to fabricate a variety of different types of devices. In turn, these devices must be chosen, designed, fabricated, and interconnected in order to construct circuits, each of which has to be designed, simulated, and built in such a way that they appropriately function when combined together with other circuit and ancillary non-circuit subsystems. Thus, this product flow path involves materials → devices → circuits → systems, with each level of the flow more than likely involving multi-feedback iterations of selection, design, simulation, fabrication, integration, characterization, and optimization.

From this perspective, devices constitute a second level of the product flow path. The multiplicity, performance, cost, manufacturability, and reliability of available device types will dictate the commercial product space in which transparent electronics technology will be able to compete. Thus, an assessment of the device toolset available to transparent electronics is of fundamental interest, and is the central theme of this chapter.

Passive, linear devices – resistors, capacitors, and inductors – comprise the first topic discussed. Passive devices are usually not perceived to be as glamorous as active devices, but

they can be enabling from a circuit system perspective, and they are also the simplest device types from an operational point-of-view. Together, these two factors provide the rationale for considering this topic initially.

Next, two-terminal electronic devices – pn junctions, Schottky barriers, heterojunctions, and metal-insulator-semiconductor (MIS) capacitors – constitute the second major topic. The motivation for this topical ordering is again associated with their relative operational complexity, rather than their utility.

The third and final major topic addressed is transistors. This is the most important matter considered in this chapter. Most of this discussion focuses on TTFTs, since they are perceived to be the most useful type of transistor for transparent electronics. Additionally, a very brief overview of alternative transistor types – static-induction transistors, vertical TFTs, hot electron transistors, and nanowire transistors – is included. This is motivated by recognizing the desirability of achieving higher operating frequencies than are likely obtainable using TTFTs with minimum gate lengths greater than ~2-10 μm, a probable lower-limit dimensional constraint for many types of low-cost, large-area applications. Alternative transistors such as these offer possible routes for reaching higher operating frequencies, in the context of transparent electronics.

4.Conclusion

Oxides represent a relatively newclass of semiconductor materials applied to active devices, such as TFTs. The combination of high field effect mobility and low processing temperature for oxide semiconductors makes them attractive for high performance electronics on flexible plastic substrates. The marriage of two rapidly evolving areas of research, OLEDs and transparent electronics, enables the realization of novel transparent OLED displays. This appealing class of see through devices will have great impact on the human–machine interaction in the near future. EC device technology for the built environment may emerge as one of the keys to combating the effects of global warming, and this novel technology may also serve as an example of the business opportunities arising from the challenges caused by climate changes The transparency of solar cells at a specific light band will also lead to newapplications such as solar windows. The field of energy harvesting is gaining momentum by the increases in gasoline price and environment pollution caused by traditional techniques.

#M. ASHWINI

(IV/IV)

CHAPTER 5: DRONES

1. Introduction

The term *unmanned aircraft system* (**UAS**) was adopted by the United States Department of Defense (DoD) and the United States Federal Aviation Administration in 2005 according to their Unmanned Aircraft System Roadmap 2005–2030.[5] The International Civil Aviation Organization (ICAO) and the British Civil Aviation Authority adopted this term, also used in the European Union's Single-European-Sky (SES) Air-Traffic-Management (ATM) Research (SESAR Joint Undertaking) roadmap for 2020.[6] This term emphasizes the importance of elements other than the aircraft. It includes elements such as ground control stations, data links and other support equipment. A similar term is an *unmanned-aircraft vehicle system* (UAVS) *remotely piloted aerial vehicle* (RPAV), *remotely piloted aircraft system* (RPAS). Many similar terms are in use.

A UAV is defined as a "powered, aerial vehicle that does not carry a human operator, uses aerodynamic forces to provide vehicle lift, can fly autonomously or be piloted remotely, can be expendable or recoverable, and can carry a lethal or nonlethal payload.

Drones are used in situations where manned flight is considered too risky or difficult. They provide troops with a 24-hour "eye in the sky", seven days a week. Each aircraft can stay aloft for up to 17 hours at a time, loitering over an area and sending back real-time imagery of activities on the ground.

Drones are seen by many in the military as delivering precision strikes without the need for more intrusive military action. However, they are not without controversy.

Unmanned aerial vehicles (UAVs), have no human pilot onboard, and instead are either controlled by a person on the ground or autonomously via a computer program. These stealth craft are becoming increasingly popular, not just for war and military purposes, but also for everything from wildlife and atmospheric research to disaster relief and sports photography. Drones are becoming the eyes and ears of scientists by surveying the ground for archaeological sites, signs of illegal hunting and crop damage, and even zipping inside hurricanes to study the wild storms. You can even rent a personal drone to soar above the horizon and snap a photo or video. Our news and features will cover developments in drone technologies, innovative uses for drones and how drone use will impact society.

2. Autonamy

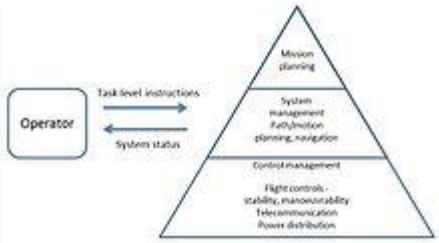


Fig.no.2

Autonomous control basics

ICAO classifies unmanned aircraft as either remotely piloted aircraft or fully autonomous. Actual UAVs may offer intermediates.

ICAO classifies unmanned aircraft as either remotely piloted aircraft or fully autonomous. Actual UAVs may offer intermediate degrees of autonomy. E.g., a vehicle that is remotely piloted in most contexts may have an autonomous return-to-base operation.

Basic autonomy comes from proprioceptive sensors. Advanced autonomy calls for situational awareness, knowledge about the environment surrounding the aircraft from exterioceptive sensors: sensor fusion integrates information from multiple sensors.

2.1. Basic principles

One way to achieve autonomous control employs multiple control-loop layers, as in hierarchical control systems. As of 2016 the low-layer loops (i.e. for flight control) tick as fast as 32,000 times per second, while higher-level loops may cycle once per second. The principle is to decompose the aircraft's behavior into manageable "chunks", or states, with known transitions. Hierarchical control system types range from simple scripts to finite state machines, behavior trees and hierarchical task planners.

Examples of mid-layer algorithms:

- Path planning: determining an optimal path for vehicle to follow while meeting mission objectives and constraints, such as obstacles or fuel requirements

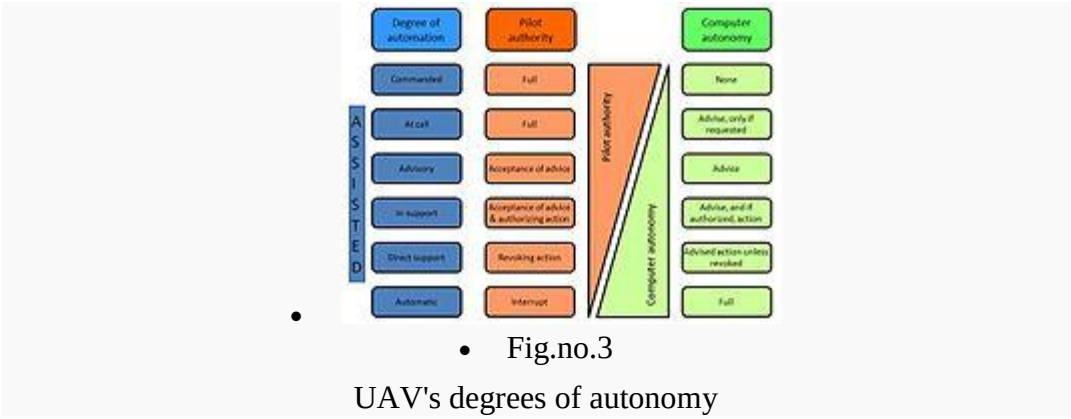
- Trajectory generation (motion planning): determining control maneuvers to take in order to follow a given path or to go from one location to another
- Trajectory regulation: constraining a vehicle within some tolerance to a trajectory

Evolved UAV hierarchical task planners use methods like state tree searches or genetic algorithms.

2.2. Autonomy features

UAV manufacturers often build in specific autonomous operations, such as:

- Self-level: The aircraft stabilizes its altitude.
- Hover: attitude stabilization on the pitch, roll and yaw axes. The latter can be achieved by sensing GNSS coordinates, called alone position hold.
- Care-free: automatic roll and yaw control while moving horizontally
- Take-off and landing
- Failsafe: automatically landing upon loss of control signal
- Return-to-home
- Follow-me
- GPS waypoint navigation
- Pre-programmed tricks such as rolls and loops



- Fig.no.3

UAV's degrees of autonomy

Quadcopter

Quadcopters generally use two pairs of identical fixed pitched propellers; two clockwise (CW) and two counter-clockwise (CCW). These use independent variation of the speed of each rotor to achieve control. By changing the speed of each rotor it is possible to specifically generate a desired total thrust; to locate for the centre of

thrust both laterally and longitudinally; and to create a desired total torque, or turning force.

Flight dynamics

Each rotor produces both a thrust and torque about its center of rotation, as well as a drag force opposite to the vehicle's direction of flight. If all rotors are spinning at the same angular velocity, with rotors one and three rotating clockwise and rotors two and four counterclockwise, the net aerodynamic torque, and hence the angular acceleration about the yaw axis, is exactly zero, which mean there is no need for a tail rotor as on conventional helicopters. Yaw is induced by mismatching the balance in aerodynamic torques (i.e., by offsetting the cumulative thrust commands between the counter-rotating blade pairs).

Flight dynamics

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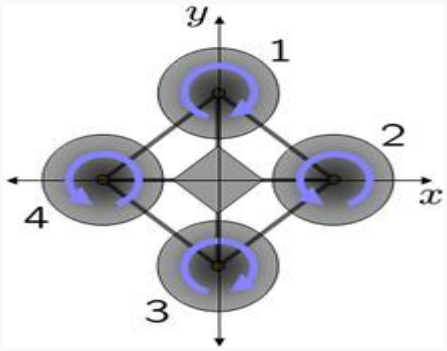
Quadrotor flight dynamics



Schematic of reaction torques on each motor of a quadcopter aircraft, due to spinning rotors. Rotors 1 and 3 spin in one direction, while rotors 2 and 4 spin in the opposite direction, yielding opposing torques for control.

Coaxial configuration

Quadcopter coaxial - OnyxStar FOX-C8 XT Observer from AltiGator

In order to allow more power and stability at reduced weight, a quadcopter, like any other multirotor can employ a coaxial rotorconfiguration. In this case, each arm has two motors running in opposite directions (one facing up and one facing down).

Vortex ring state

All quadcopters are subject to normal rotorcraft aerodynamics, including vortex ring state.

Mechanical structure

The main mechanical components needed for construction are the frame, propellers (either fixed-pitch or variable-pitch), and the electricmotors. For best performance and simplest control algorithms, the motors and propellers should be placed equidistant. Recently,carbon fiber composites have become popular due to their light weight and structural stiffness.

The electrical components needed to construct a working quadcopter are similar to those needed for a modern RC helicopter. They are the electronic speed control module, on-board computer or controller board, and battery. Typically, a hobby transmitter is also used to allow for human input.

Autonomous flight

Quadcopters and other multicopters often can fly autonomously. Many modern flight controllers use software that allows the user to mark "way-points" on a map, to which the quadcopter will fly and perform tasks, such as landing or gaining altitude. The PX4 autopilot system, an open-source software/hardware combination in

development since 2009, has since been adopted by both hobbyists and drone manufacturing companies alike to give their quadcopter projects flight-control capabilities. Other flight applications include crowd control between several quadcopters where visual data from the device is used to predict where the crowd will move next and in turn direct the quadcopter to the next corresponding waypoint.

3.Conclusion

It can be concluded from the above discussion that as with other man made technologies this technology is also not without its benefits and drawbacks.

• The need of the time is to research upon its advantages rather than disadvantages. However the mass murder of humans using this technology should be put to a halt as soon as possible.

• The UN's Special Rapporteur on extrajudicial, summary or arbitrary executions, Philip Alston, has said that the use of drones is not combat as much as 'targeted killing'. • He has repeatedly tried to get the US to explain how they justifies the use of drones to target and kill individuals under international law.

#B. SATHWIKA

(IV/IV)

CHAPTER 6:

NAND FLASH MEMORY WITH MULTIPLE PAGE SIZES FOR HIGH-PERFORMANCE STORAGE DEVICES

1. INTRODUCTION

Flash memories are divided into two main categories as NOR flash is more suitable for code execution due to low read latencies, NAND flash are commonly used for data storage. In this document we focus on NAND flash. It is today the main building block for secondary storage systems in embedded systems. This popularity is due to its many benefits: high data density, good I/O performance, shock resistance, and low power consumption. Some of these benefits are due to the fact that flash is entirely composed of electronic components, compared to hard drives containing mechanical parts.

Nevertheless, NAND flash memories (referred as “flash memory” in the rest of this document) are prone to specific constraints, due to their internal intricacies: the impossibility to perform in-place data updates, the erase/write operation asymmetry, and the limited lifetime of the memory cells. These drawbacks bring the need for specific flash management in the systems integrating such memories. This management can be provided in a software layer by the operating system through dedicated Flash File Systems (FFSs).

A performance evaluation for FFS allows us to understand the behavior of such systems, and also to know how to choose the best FFS for a given hardware/software context. We can also highlight some particular points of interests in the FFS behavior, for example in order to propose optimizations.

Storage devices based on NAND flash memory (NFM), e.g. solid-state disks (SSDs), are rapidly widening their market share thanks to superior characteristics of NFM such as faster access speed, stronger shock-resistance, and lighter weight than conventional magnetic disks. Besides SSDs, NAND flash-based storage devices (NFSDs) are used in USB memory sticks, portable/mobile devices, etc. As many manufacturers continuously reduce the cost-per-bit gap between NFSDs and conventional non-volatile storage devices, e.g. HDD, NFM becomes dramatically denser and cheaper.

From a system perspective, however, NFSDs based on denser NFM chips only reduce the cost but does not necessarily improve the performance of system. It shows the trend of two different design objectives, performance and cost, as the NFM technology advances. Released year, page size, number of pages per block for several generation of NFM chips are

provided under the x-axis and they reflect the current technology trend, which increases the size of a page and the number of pages within a block. The cost in the figure is continuously decreasing as technology advances. However, the performance represented by throughput, shows two different trends with respect to the applications running on the NFSD. This indicates that the increased size of pages and blocks may be harmful under certain applications.

This measurement clearly questions a conventional wisdom that the cheaper and denser NFM thanks to advance in technology is helpful to satisfy various design objectives of NFSDs. In other words, the increased page and block sizes successfully reduce cost-per-bit of NFSDs but their effects on the performance are different from applications to applications. For this reason, to really understand the system-level impact of technology advance in NFM, we need to analyze the design parameters, i.e. specification of NFM, and the characteristics of applications and understand how they affect the system-level objectives of NFSDs.

2.NAND FLASH MEMORY

NAND flash-based storage devices (NFSDs) have dramatically increased the demand for compact and reliability. NAND flash memory (NFM) offers many advantages, such as non-volatility, high performance, the small form factor, and low-power consumption, while rapidly improving capacity and cost by downscaling the process technology to 21 nm and providing a 3-D NFM structure.

NFM's higher degree of chip integration compared with other types such as NOR flash memory is achieved by its specialized architecture for bulk data access. In this architecture, the page the unit for read and program operations includes numerous memory cells. The unit for erase operations, the block, is composed of tens of pages. Page size has continuously increased since early NFMs, when a single page was smaller than 1 kB.

Increasing the page size enlarges the portion of cell areas in a die and reduces the number of NFM operations that service a given amount of data. Thus, the larger page reduces the cost-per-bit of NFMs and improves the throughput of NFSDs. However, the larger page cannot guarantee better performance in all cases. In particular, the larger page causes higher fragmentation within NFMs, which causes inefficient utilization of NFM space [called false capacity (FC)] and increases the number of garbage collections (GCs). Moreover, when requests with a small amount of data are given, NFM write performance

deteriorates because of frequent read-and-modify procedures.

Despite the limitations, increasing the page size is inevitable because of its cost reduction and the performance bottlenecks caused by large requests. We, therefore, propose an NFM architecture that offers the advantages of a small page without sacrificing the benefits of a large one. Although discussed the necessity of such architecture, they did not propose specific and realistic solutions for the implementation.

The contributions of this brief can be summarized as follows. First, we propose a multiple page size NFM (MPNFM) architecture. These multiple page sizes occur within a die without affecting the area and manufacturing process. In addition, the implementation is simple, because only some logics are shifted to generate the differential page sizes.

Second, a management method for effectively utilizing NFSDs equipped with the MPNFM is proposed. The related algorithm cooperates with any existing flash translation layer (FTL), the software layer that manages NFM. The proposed method retains the sophisticated features of the existing FTLs and adds certain modules to maximize the MPNFM effects. According to our experiments, the combination of MPNFM and the management algorithm greatly improves write performance compared with single-page-size NFM (SPNFM).

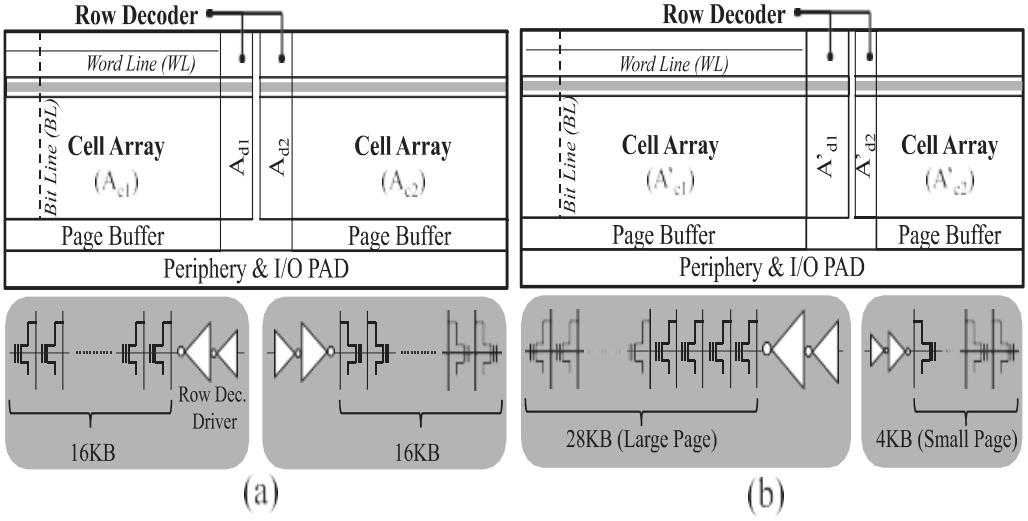


Fig 2.1: (a) SPNFM (b) MPNFM

To elucidate the advantages of MPNFM, we use a simple example with three different NFMs, as shown in Fig. 2: 1) SPNFM with small pages (SPNFM-S); 2) SPNFM with large pages (SPNFM-L); and MPNFM. The smallest represents a sector (512 B); the block size of all NFMs is 2 kB.

The numbers of pages and page sizes among the three NFMs differ. One block of

SPNFM-S includes four small pages, and a page consists of one sector, whereas one block of SPNFM-L includes one large page comprised of four sectors. The gray areas represent unusable portions because of the impossibility of in-place updates. The number of gray areas is proportional to the amount of FC.

For Request 1, SPNFM-S and MPNFM require only one NFM program, whereas SPNFM-L requires an additional NFM read for read-and-modify operations. When a page needs to be modified, NFM can write new data only after moving some old data in the page into a new page in order to preserve the old data not changed by the new request. This is called read and modify. This means that the NFM that utilizes smaller pages is more suitable for small writes. Cumulative read and modify procedures can significantly degrade write performance. Request 2 is a sequential read request that fetches three sectors. When Request 2 is given, SPNFM-L and MPNFM, which include large pages, outperform SPNFM-S, which has only small pages, because of the higher throughput caused by the large pages. This difference is additionally demonstrated by sequential write requests.

A small page typically issues more program commands than larger pages therefore, its throughput is lower than that of larger pages. In addition, the page size difference shows significant effects after the two requests are serviced. As described above, the gray boxes denote portions of pages that cannot be written without an erase operation (i.e., FC). Large FC, which is caused by fragmentation, increases the frequency of GC. After two requests, the FC values of SPNFM-S, SPNFM-L, and MPNFM. In other words, SPNFM-L is the first NFM type requiring GC because of its low efficiency in utilizing pages. The aforementioned advantages of MPNFM are effective only if the workloads given to NFMs have both sequential and random requests sufficient for contributing to NFSD performance. We analyzed I/O characteristics of several workloads, shows that the request size in various workloads had two different aspects.

3.Flash Translation Layer (FTL)

A flash translation layer (FTL) is a software layer used by many NFSDs to fill the gap between conventional file systems and NFM based file systems. It serves multiple roles such as address translation, garbage collection, and wear-leveling, each of which is closely related with the design objectives of NFSDs.

Most address translation schemes of FTL are based on a mapping table between logical and physical addresses and the granularity of the mapping table is one of the most important factors for the overall performance of NFSDs. Due to the limited size of volatile

memories, either caching the mapping table during execution of the FTL or a hybrid-level FTL has been proposed, which combines a cheap but limited-performance block mapping method and a costly but good-performance page mapping method.

A garbage collection scheme is also a crucial factor for the performance of NFSDs since it dictates the number of valid page copy and erase operations of NFM. Most FTL schemes have focused on implementing effective garbage collection.

Wear-leveling is an algorithm developed to extend the limited life-time. The life-time is determined by the number of erase operations experienced by a block of the NFM. A block guarantees its functionality until it experiences a fixed number of erase operations. The total number of erase operations decreases as the number of bits stored within a cell increases.

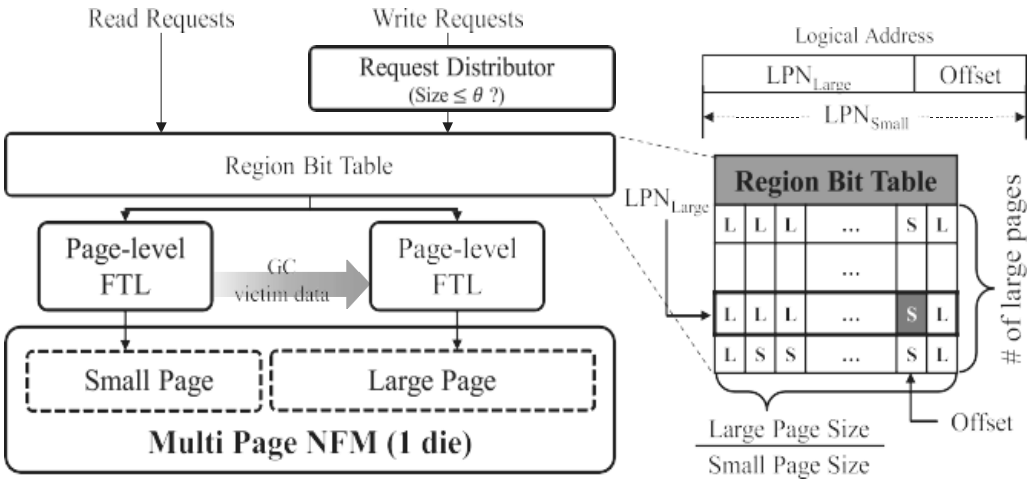


Fig 4.1: Flash Translation Layer

4.CONCLUSION

We analyze various design parameters in the specifications of NFM and show optimizing these parameters has a big impact on performance, cost, and power of NFSD. Our simulations show that unfortunately recent trends in NFM specifications toward denser cells and larger page and block sizes focus on cost reduction and adversely affect the performance and power consumption. In addition, we show optimizing design parameters to meet specific design objectives of NFSD requires understanding of the characteristics of applications.

These results can be utilized to choose optimal design parameters in NFM specifications for given applications, e.g. embedded applications with specific request patterns. Alternatively, we could use the results to design future specifications of NFM.

As a future work, we may use our exploration results to design an application-specific storage device with heterogeneous NFMs. Since each hierarchy of NFM should experience different access patterns, the optimal types of NFMs would be easily derived from the results of this paper.

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CHAPTER 7:

MINIMIZATION OF VLSI FLOORPLAN USING HYBRID PSO

1.INTRODUCTION

Floorplanning is becoming more important for very large-scale integration (VLSI) physical design. Floorplanning is the process of planning the arrangement of modules in such a manner that area and interconnection wire length should be minimized. According to Moore's Law, the number of transistors gets doubled for every eighteen months. This results in increasing the complexity of the circuits. The feature size of the IC is considerably scaled down, which results in an increase in search complexity. This makes the IC design more complex and corresponds to NP Hard Problem. Floorplanning can be represented by using a different approach such as graph-based, tree based or sequence-based representation. VLSI floorplanning is an NP-Hard problem and it can be solved using heuristic and meta-heuristic algorithm. Genetic algorithm has been proved to be an efficient method to solve VLSI floorplanning. Another heuristic algorithm, Particle Swarm Optimization can also be applied to solve NP-Hard Problem and VLSI floorplan experimental results prove that PSO has better searching ability than Simulated Annealing (SA). The advantage of the PSO algorithm is that it avoids falling into local minimum and exhibits a rapid convergence rate. The main drawback of the PSO algorithm is that it has weak local search ability. In order to overcome this drawback, PSO algorithm is hybridized with Cuckoo search algorithm

2.FLOORPLANNING

2.1 Floorplanning:

Floorplanning is the process of planning the arrangement of modules in such a manner that area and interconnection wirelength should be minimized.

Floorplanning is the first major step in physical design; it is particularly important because the resulting floorplan affects all the subsequent steps in physical design, such as placement and routing.

Floorplanning provides early feedback that:

- evaluates architectural decisions,
- estimates chip areas, and
- estimates delay and congestion caused by wiring.

Two popular approaches to floorplanning are:

1. **Simulated annealing:** simulated annealing- based floorplanning relies on the representation of the geometric relationship among modules
2. **Analytical formulation:** an analytical approach usually captures the absolute relationship directly.

The representation of geometric relationship is done using three popular floorplan representations:

1. normalized Polish expression
2. B*-tree
3. Sequence Pair

These representations are efficient, flexible, and effective in modeling geometric relationships (e.g., left, right, above, and below relationships) among modules for floorplan designs.

2.2 Problem Statement:

Let M be the set of modules represented by M= {m1, m2….mN}, where N is the number of modules. Each module mi is represented by (Wi, Hi), where $1 \leq i \leq N$, Wi is width of the module mi and Hi is the height of the module mi. The aspect ratio of mi is defined as Hi / Wi . The area Ai of the module mi is given by Wi*Hi

The goal of floorplanning is to optimize a predefined cost metric such as a combination of the area (i.e., the minimum bounding rectangle of F) and wire length (i.e., the sum of all interconnection lengths) induced by a floorplan. For modern floorplan designs, other costs such as rout ability, power, and thermal might also need to be considered.

2.3 Floorplanning model:

Two categories for discussions, they are given by:

1. Slicing floorplanning
2. Non slicing floorplanning

2.3.1 Slicing Floorplanning:

A slicing floorplan can be obtained by repetitively cutting the floorplan horizontally or vertically.

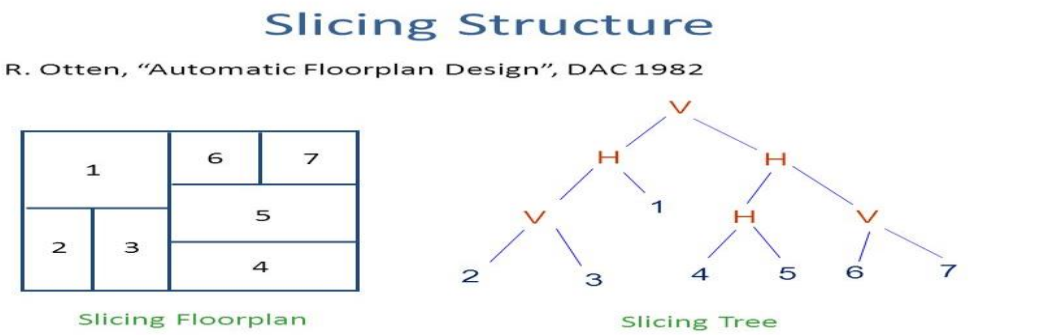

Fig:(a) slicing floorplanning **fig(b) slicing tree (or)binary tree**

Figure : Slicing floorplanning

We can use a binary tree to represent a slicing floorplan. A slicing tree is a binary tree with modules at the leaves and cut types at the internal nodes. There are two cut types, H and V. The H cut divides the floorplan horizontally. Similarly, the V cut divides the floorplan vertically. Slicing floorplan may correspond to more than one slicing tree, because the order of the cut-line selections may be different.

2.3.2 Non-Slicing Floorplanning:

Non slicing floorplan is more common than slicing floorplan. All the children of the given cell cannot be obtained by bisecting the floorplan. This is called non-slicing floorplan. Horizontal constraint graph and vertical constraint graph can be used to model a non-slicing floorplan. In a constraint graph, a node represents a module.

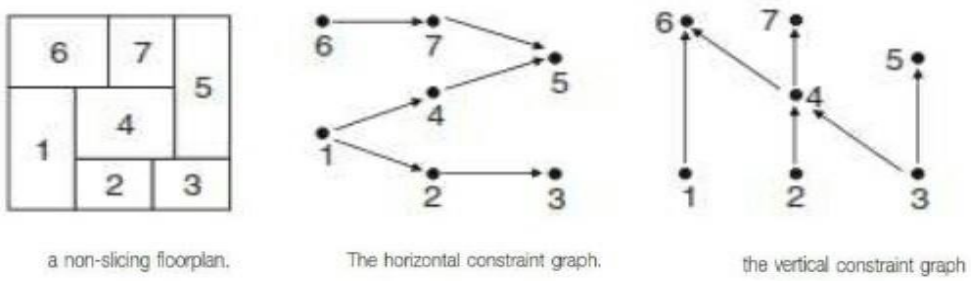

Fig:(a) **fig:(b)** **fig:(c)**

Figure : Non slicing floorplanning

figure(a) represents non slicing floorplan, and Fig(b) and Fig(c) shows vertical and horizontal constraint graph of Fig(a) respectively.

We use a horizontal constraint graph (HCG) and a vertical constraint graph (VCG) to model a non-slicing floorplan. The horizontal constraint graph defines the horizontal relations of modules, and the vertical constraint graph defines the vertical ones. In a constraint graph, a node represents a module. If there is an edge from node A to node B in the HCG (VCG), then module A is at the left (bottom) of module B.

Several representations of non-slicing floorplan are corner sequence, corner block list, O tree, sequence

3.PARTICLE SWARM OPTIMIZATION (PSO)

3.1 Particle Swarm Optimization (PSO):

PSO is a population based optimization method and it can be used to optimize a problem by several iterations in order to improve a candidate solution with regard to quality. PSO optimizes a problem by using a population of candidate solutions (from corner list). Each particle represents an individual in the population. By adopting PSO algorithm, the particles are moved around in the search-space according to the particle's position and velocity. The particle's best position so far is said to be pBest. The best of pBest value among all the particles is considered as gBest. The velocity and position of each particle is updated according to the following equations.

$$V_{t+1} = W_t * V_t + C1 * rand( ) * (pBest - X_t) + C2 * rand( ) * (gBest - X_t) \quad \text{(3)}$$

$$X_{t+1} = X_t + V_{t+1} \quad \text{(4)}$$

where t is the iteration index, W is the inertia weight, C1and C2 are two positive constants, called acceleration constants, rand( ) is random function within the range [0,1].The new velocity of each particle is calculated by using equation (3) based on its previous velocity and the personal best location and the global best location of the population. The particle's position is updated by using equation (4).

Acceleration coefficient of each particle is calculated using equation (5) and (6).

$$C1 = cIter * (c1e - c1s)/MAXITER + c1s \quad \text{(5)}$$

$$c2 = cIter * (c2e - c2s)/MAXITER + c2s \quad \text{(6)}$$

where cIter is the current iteration number and MAXITER is the maximum number of allowable iteration, c1e, c2e represent the final value of the c1 and c2 and c1s, c2s represent the initial values of the c1 and c2

3.2 Flowchart of PSO based CL:

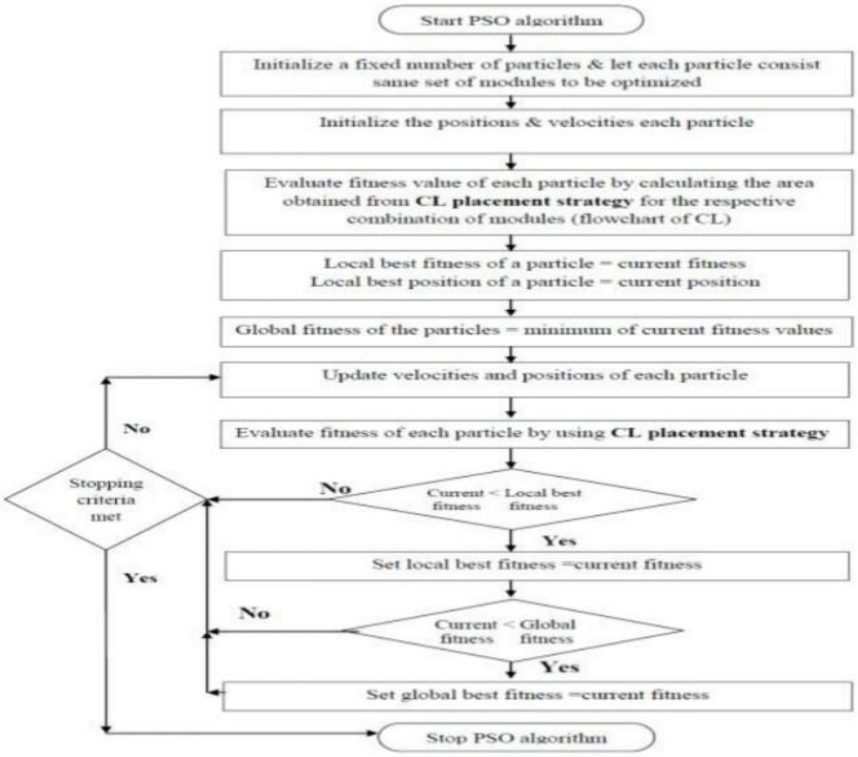

Figure : flowchart of PSO based CL

The pseudo code of the PSO is as follows:

1. Create and initialize a corner list and particle
2. Repeat until maximum iterations
3. For each particle, Calculate fitness value from corner list ,
4. If fitness value is better than pBest ,
5. Set fitness value as pBest,
6. Choose gBest from pBest of all particles,
7. Calculate the particle velocity by using equation (3)
8. Update the particle position by using equation (4)
9. End.

3.3 Floorplanning based on PSO:

STEP 1: Load the modules input and initialize the parameter of the PSO algorithm.

STEP 2: Generate an initial population, initialize the position and velocity of each particle, and calculate the Pbest of each particle and the Gbest population.

STEP 3: Calculate the fitness value of each particle by equation (3) and (4)

STEP 4: Check each particle, if its fitness value is better than Pbest, update its Pbest with the fitness value.

STEP 5: Check each particle, if its fitness value is better than population's Gbest, update its Gbest with the fitness value.

STEP 6: Adjust the position and velocity of each particle according to equations (1) and (2)
STEP 7: If termination condition is satisfied, the algorithm stops; otherwise, go to step 3.

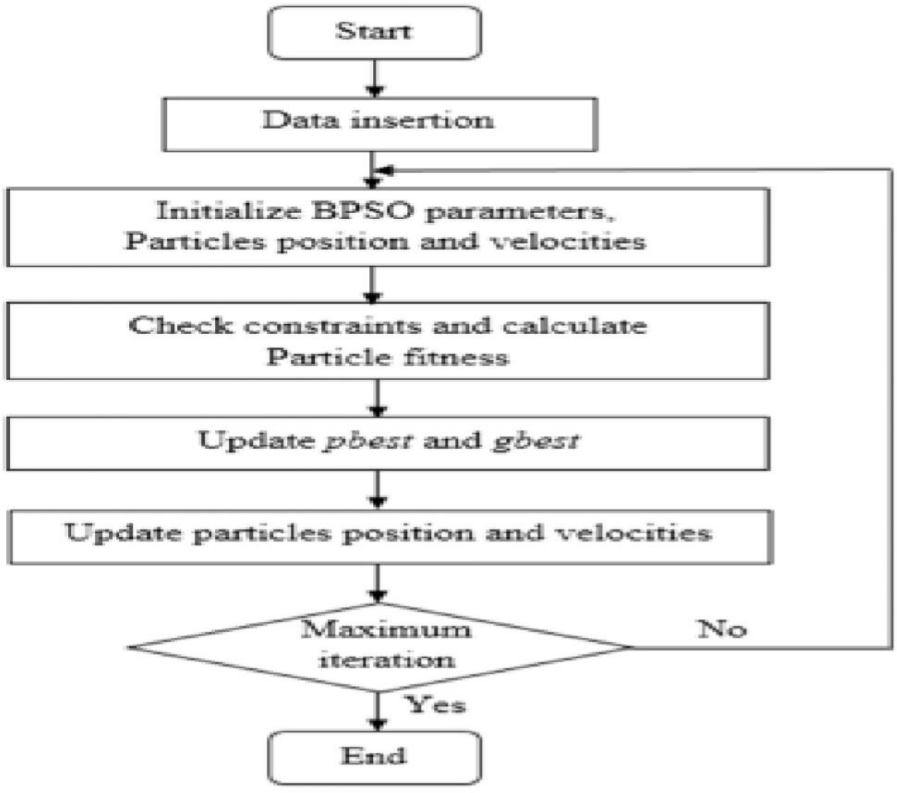

Figure : Floorplanning based on PSO

3.4 Area and wirelength minimization: For multiobjective optimization, both area and interconnection wirelength should be minimized simultaneously. The fitness function for both area and wirelength optimization is given by,

$$y(x) = \alpha * f(x) + \beta * g(x) \ldots\ldots\ldots\ldots (7)$$

where α and β are constant weight values in the range of 0 to 1, f(x) represents the area of the particle x, g(x) represents the wirelength of particle x. The wirelength of particle x is calculated by using Half-Perimeter Wire Length (HPWL). The HPWL of the net k is calculated by using the following formula:

$$Lp = (Xmax - Xmin) + (Ymax - Ymin) \ldots\ldots\ldots\ldots (8)$$

where Xmax and Xmin denotes the maximum and minimum x- coordinates of the HPWL bounding box of the net. Ymax and Ymin represents the maximum and minimum y-coordinates of the HPWL bounding box of the net. The total wirelength can be estimated by using the following equation:

$$(\square) = \sum \square\square\ \square\ \square = 1 \ldots\ldots\ldots\ldots\ldots (9)$$

The simulation results of optimized area and wirelength of MCNC Benchmark circuits are shown in the Fig.1,2,3,4 respectively.

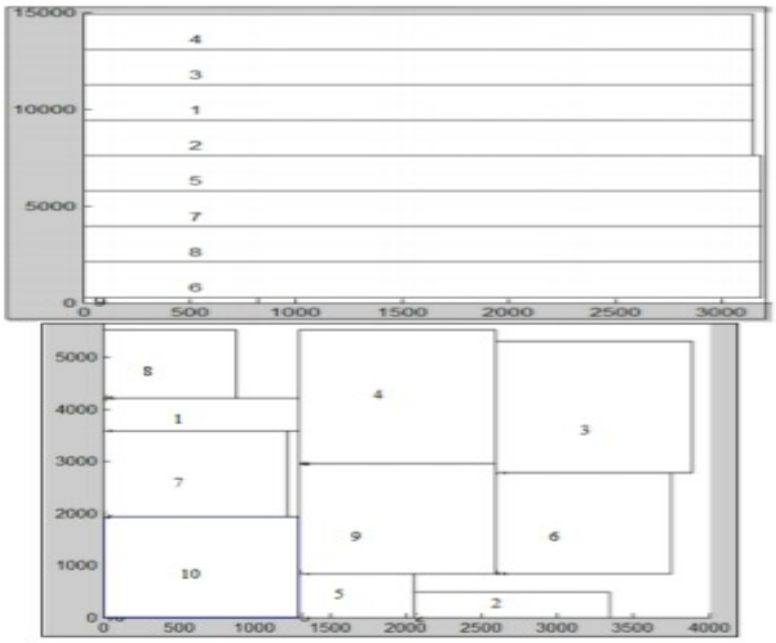

Figure: Simulation result on MCNC apte and MCNC xerox

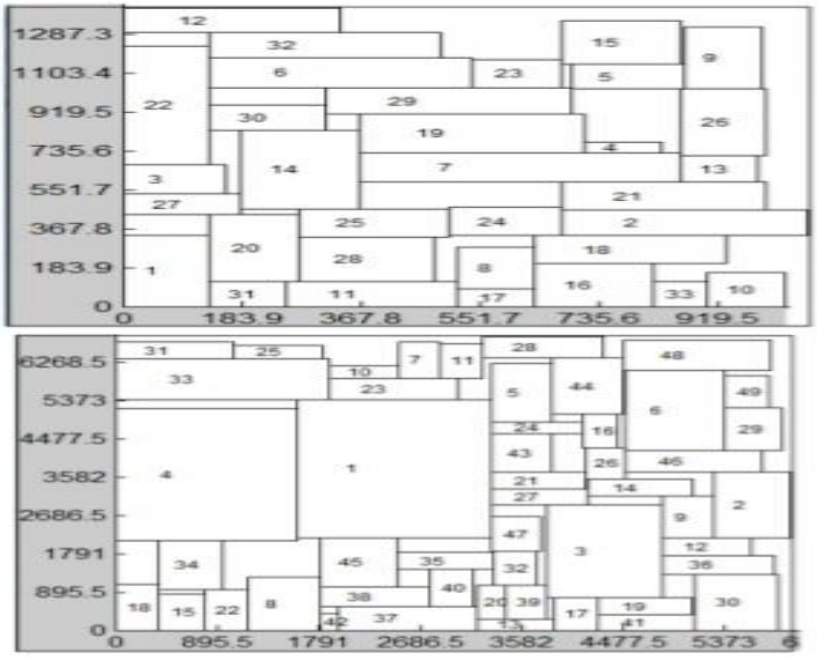

Figure: Simulation result on MCNC ami33 and MCNC ami49

4.CONCLUSION

1. In this seminar, PSO algorithm in order to solve nonslicing floorplan in efficient manner.
2. Corner list representation is a new floorplan representation and it is used to represent non-slicing floorplan.
3. The experimental results for MCNC benchmark circuits demonstrated that the proposed algorithm can able to achieve the optimal result for hard modules placement. The future work will focus on the parameter related to some constraints.

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CHAPTER 8: HIGH SPEED 16x16 BIT AREA EFFICIENT MODIFIED VEDIC MULTIPLIER

1.INTRODUCTION

Multiplication is an important fundamental function in arithmetic operations. Multiplication- based operations such as Multiply and Accumulate(MAC) and inner product are among some of the frequently used Computation- Intensive Arithmetic Functions(CIAF) currently implemented in many Digital Signal Processing (DSP) applications such as convolution, Fast Fourier Transform(FFT), filtering and in microprocessors in its arithmetic and logic unit. Since multiplication dominates the execution time of most DSP algorithms, so there is a need of high speed multiplier. Currently, multiplication time is still the dominant factor in determining the instruction cycle time of a DSP chip.

The demand for high speed processing has been increasing as a result of expanding computer and signal processing applications. Higher throughput arithmetic operations are important to achieve the desired performance in many real-time signal and image processing applications. One of the key arithmetic operations in such applications is multiplication and the development of fast multiplier circuit has been a subject of interest over decades. Reducing the time delay and power consumption are very essential requirements for many applications. This work presents different multiplier architectures. Multiplier based on Vedic Mathematics is one of the fast and low power multiplier. Minimizing power consumption for digital systems involves optimization at all levels of the design. This optimization includes the technology used to implement the digital circuits, the circuit style and topology, the architecture for implementing the circuits and at the highest level the algorithms that are being implemented. Digital multipliers are the most commonly used components in any digital circuit design. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application.

The multiplier is a fairly large block of a computing system. The amount of circuitry involved is directly proportional to the square of its resolution i.e. A multiplier of size n bits has n2 gates. For multiplication algorithms performed in DSP applications latency and throughput are the two major concerns from delay perspective. Latency is the real delay of computing a junction, a measure of how long the inputs to a device are stable is the final

result available on outputs. Throughput is the measure of how many multiplications can be performed in a given period of time; multiplier is not only a high delay block but also a major source of power dissipation. That‟s why if one also aims to minimize power consumption, it is of great interest to reduce the delay by using various delay optimizations.

In this, Urdhva tiryakbhyam Sutra is first applied to the binary number system and is used to develop digital multiplier architecture. This is shown to be very similar to the popular array multiplier architecture. This Sutra also shows the effectiveness of to reduce the NXN multiplier structure into an efficient 4X4 multiplier structures. The proposed multiplication algorithm is then illustrated to show its computational efficiency by taking an example of reducing a 4X4-bit multiplication to a single 2X2-bit multiplication operation . This work presents a systematic design methodology for fast and area efficient digit multiplier based on Vedic mathematics .The Multiplier Architecture is based on the Vertical and Crosswise algorithm of ancient Indian Vedic Mathematics.

2.ARRAY MULTIPLIER

The traditional method for multiplication is doneby using Array multiplier. Array multiplier is popular due toits familiar structure as it is based on add and shift algorithm. In Array multiplication operation, number of partial products to be added is the main parameter that determines the performance of the multiplier. Each partial product is generated by the multiplication of the multiplicand with one multiplier bit. These products are added systematically by shifting operation .There will be a shift in partial roducts after the multiplication of one bit of multiplier with multiplicand. After the multiplication process of all the multiplicand bits with all the multiplier bits, the final step is to add all the partial products to get the result. For this firstly group the partial products in order of two rows each and the products which fall under same group are added by using conventional half and full adders and their respective carries are passed on to next stages. The result from the first step is then added to the next row of partial products. The same procedure is followed until final output is obtained. Representation of 8*8 array multiplier is shown in Figure. Here the multiplication process of multiplicand (8bits) with multiplier (8bits) using Array multiplier is shown. The output as 16bits in which 15 bits are sum bits and one carry bit is obtained.

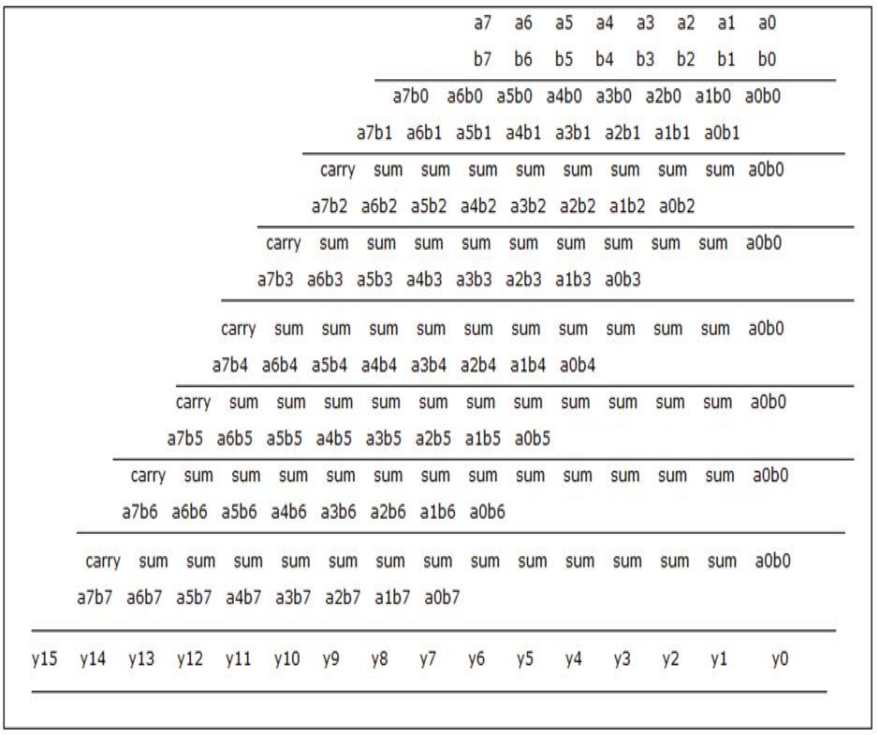

Fig .Array multiplier for 8bit

3.Vedic Multiplier

The main purpose of Vedic Mathematics is to be able to solve complex calculations by simple techniques. The formula being very short makes them practically simple in implementation. Urdhva-tiryagbhyam (Vertically and crosswise) sutra is general formula applicable to multiplication operation**.** The strategy applied for developing a 64 x 64-bit Vedic multiplier is to design a 2 x 2- bit Vedic multiplier as a basic building module for the system. In the next stage of development a 4 x 4-bit multiplier is designed using 2 x 2- bit Vedic multiplier. Further in same manner 8 x 8,16 x 16 and32 x 32- bit Vedic multiplier is designed. For the partial product addition for all stages of development a fast adders is used. Multiplier plays a very important role in today's digital circuits. The multiplier is based on an algorithm Urdhva Tiryagbhyam (Vertical and crosswise).This sutras shows how to handle multiplication of larger number (N X N bits) by breaking it into smaller sizes.

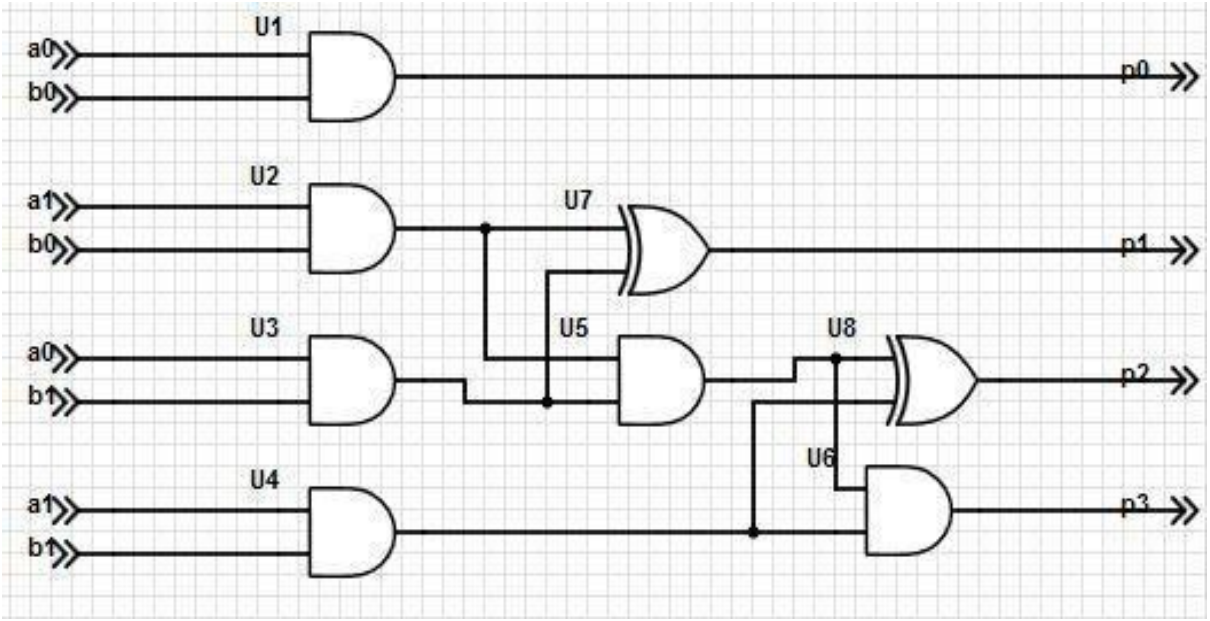

FIG . DESIGN OF 2X2 URDHVATIRYAKBHAYAM VEDIC MULTIPLIER ARCHITECTURES

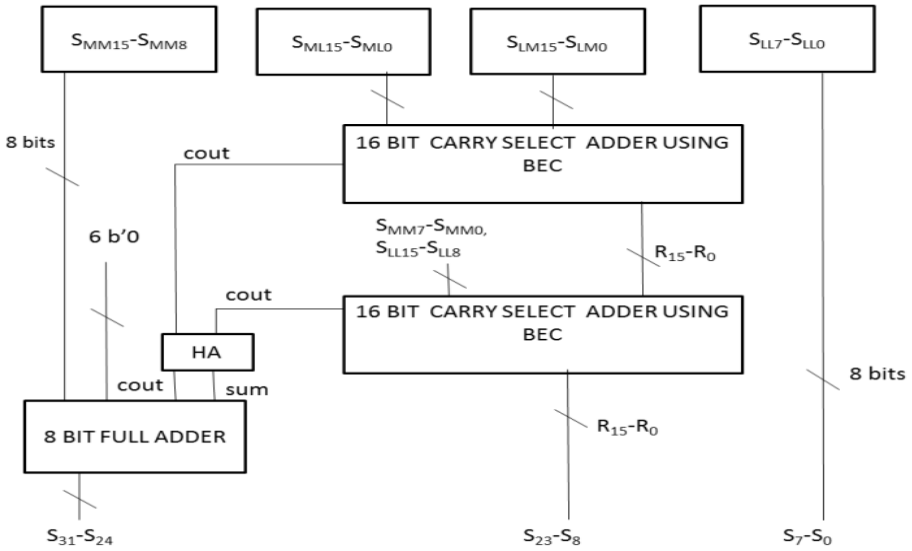

FIG : 16x16 VEDIC MULTIPLIER USING BEC:

The design of 4x4 Vedic multiplier is used as abasic building block diagram for design of 8x8 Vedic multiplier. Further design of 16x16 is implemented by using8x8. Vedic multiplier as basic building block. The aim ofusing BEC is to reduce the usage of gates compared to normal Vedic multiplier which in turn reduces the powerconsumption.

The structure of proposed Vedic multiplier isshown in figure 6. It has 4 groups of same size i.e eachgroup consists of 8*8 Vedic multiplier whose inputs are partitioned

according to Urdhva-tiryagbhyam sutra. Outputs from Vedic multiplier are given as inputs to BEC adders ofdifferent sizes.

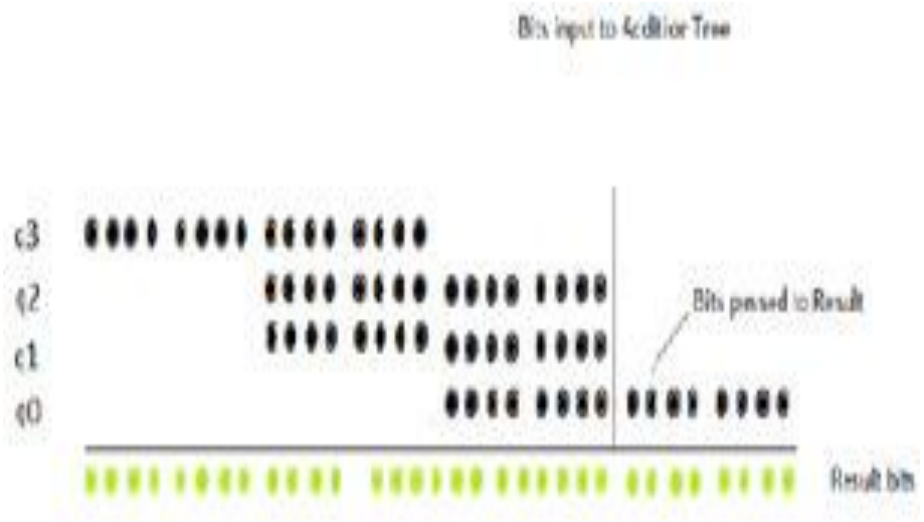

FIG. Multiplication process of 16x16 multiplier

4.CONCLUSION:

- From the above results it is clear that for 8bit, memory utilized for Vedic multiplier using BEC (138728KB) is less when compared to Vedic multiplier (198568KB).
- In the case of 16bit vedic multiplier, memory utilized or Vedic multiplier using BEC (139624KB) is less when compared to normal Vedic multiplier (208268KB).
- By comparing the values of both Array and Vedic multiplier it is clear that the delay

for Vedic multiplier is much less when compared with Array multiplier. As increase number of bits delay can be reduced by using Vedic multiplier than Array multiplier.

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